

Big Ben Strikes Again

Hear the distinctive chimes of Big Ben strike the quarter hours in this digital clock that uses a single, PSoC chip. The PSoC synthesizes a natural, mechanical chime melody of the famous “Big Ben” clock in London’s Victoria Tower. This melody is taken from a composition by Handel, “I Know My Redeemer Liveth.”

Each chime note is synthesized by the PSoC, generating the pitch, timbre, and loudness contour of the desired note. For example, a chime note has the pitch or dominate frequency of A5 (440 Hz). The timbre is accomplished by properly mixing the fundamental or “strike” frequency of A5 with the related note frequencies: A6 (880 Hz), the second harmonic; E6 (1318.8 Hz), the major fifth; and C5 (523.3 Hz) the minor third. The loudness contour is the percussive shape of fast attack and immediate, exponential decay.

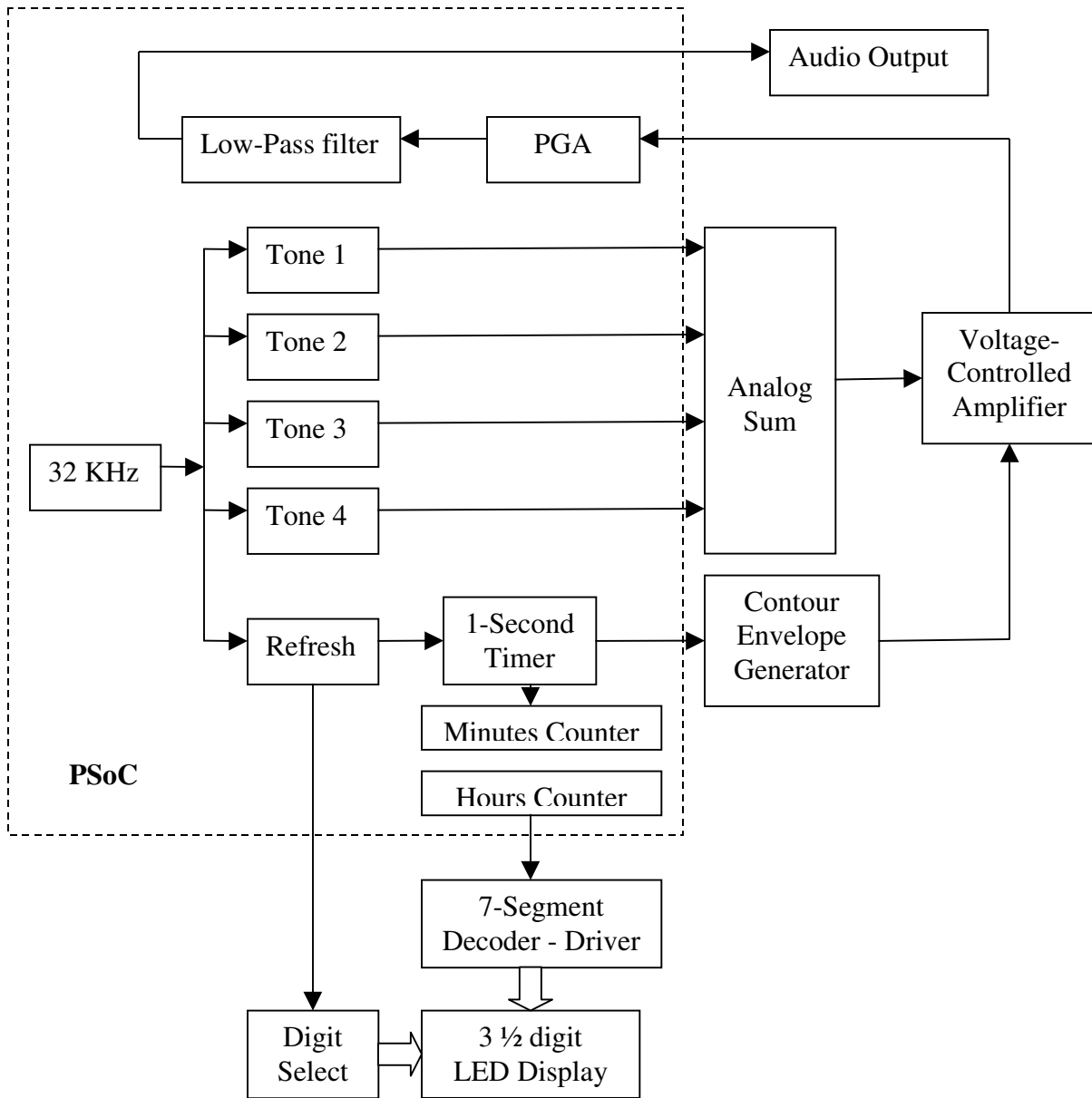
All five of the chime notes used to produce the Westminster Chimes melody are synthesized in this manner, four notes for the melody and one note for the striking hour. Four 8-bit PWM counters are used to generate each chime note. The PWM control registers are reset to the next chime note values in order to play the entire melody. The digital outputs of the four PWM counters are applied to a resistor-summing network and applied to a voltage-controlled amplifier. The volume contour control-voltage envelope is an exponential-decay and is developed from the 1-second timer digital output driving a simple, resistor-capacitor network. This volume contour is applied to each chime note.

The chime note with its proper volume contour envelope is then fed back to an analog input Programmable Gain Amplifier (PGA) block in the PSoC. The analog audio signal is then sent through a 2-pole, low-pass filter (LPF) block. The corner frequency of

Entry #280

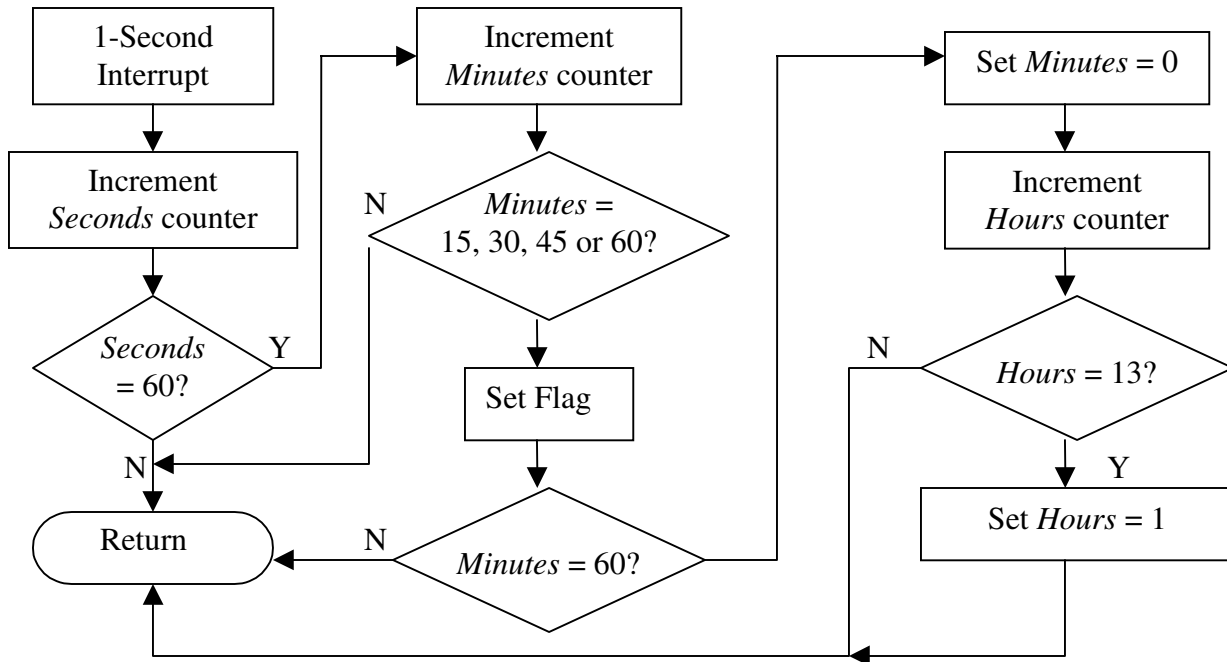
this LPF is fixed at 1 KHz and removes the remaining, higher harmonic frequencies from the square-wave PWM signals. The filtered, analog audio output signal is available on the PSoC PORT 0_5 analog output pin.

The digital clock is derived from the PSoC's internal 32 KHz clock which generates both a 1-second interrupt and the multiplex control for the LED clock display. The minutes and hours counters are maintained as software registers inside the PSoC. LED display is refreshed by the PSoC at a rate of 112 Hz in an interrupt service routine.



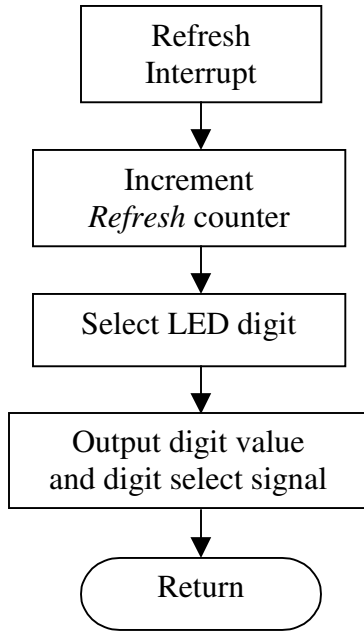
Big Ben Block Diagram

Almost all of the work is done inside of the PSoC. Only a small amount of analog circuitry and the LED display are needed to make Big Ben complete.



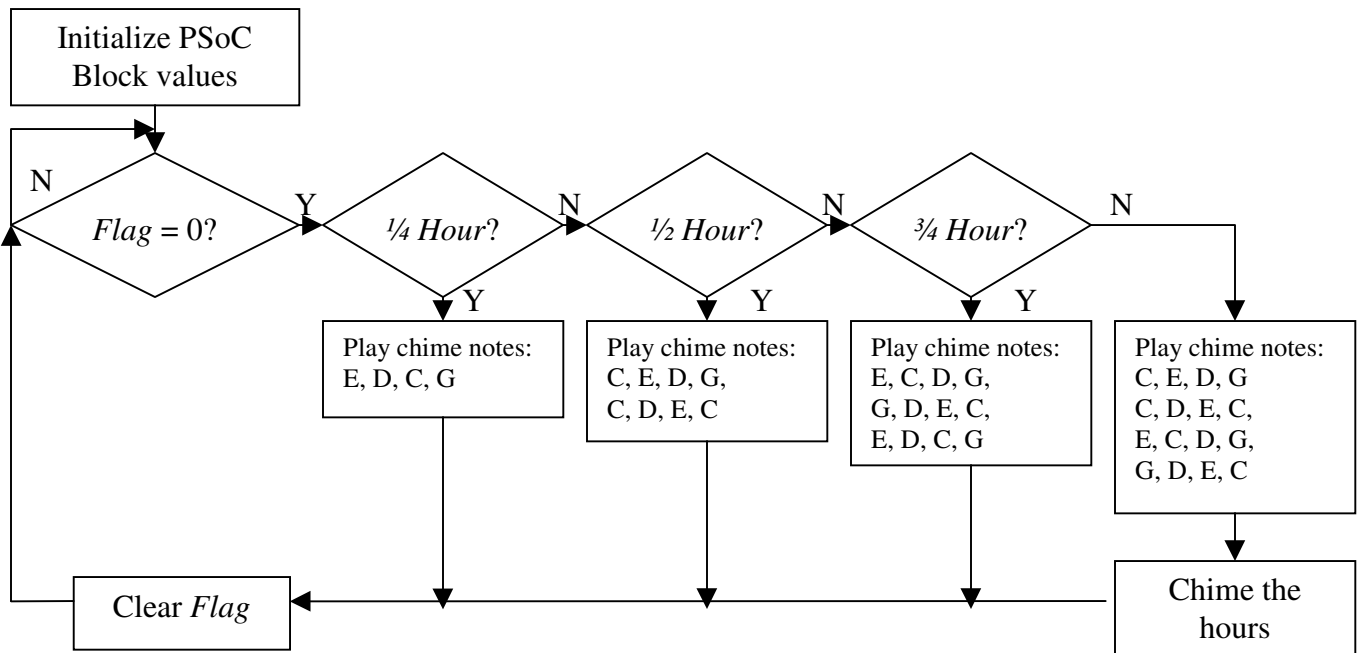
Big Ben 1-Second Interrupt Service Routine

The hard work is done in the 1-Second ISR which keeps the time and flags the main-line code when it is time to chime the quarter hours and the hours.



Refresh Interrupt Service Routine

The Refresh ISR simply selects one of the four clock digits (hours or minutes) and outputs the current clock value to the LED display along with the digit select signal.



Main-line code

