

Programmable Signal Generator

Objective

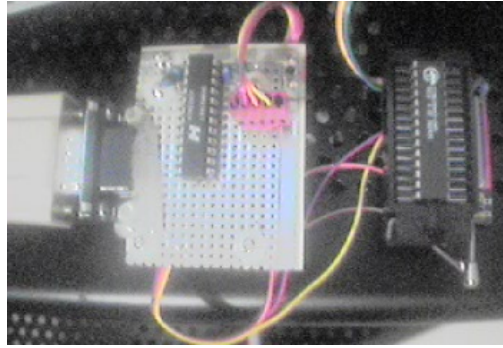
Create a benchtop programmable signal generator capable of generating a sine, triangular and square waves based upon commands received on the RS232 port.

Specifications

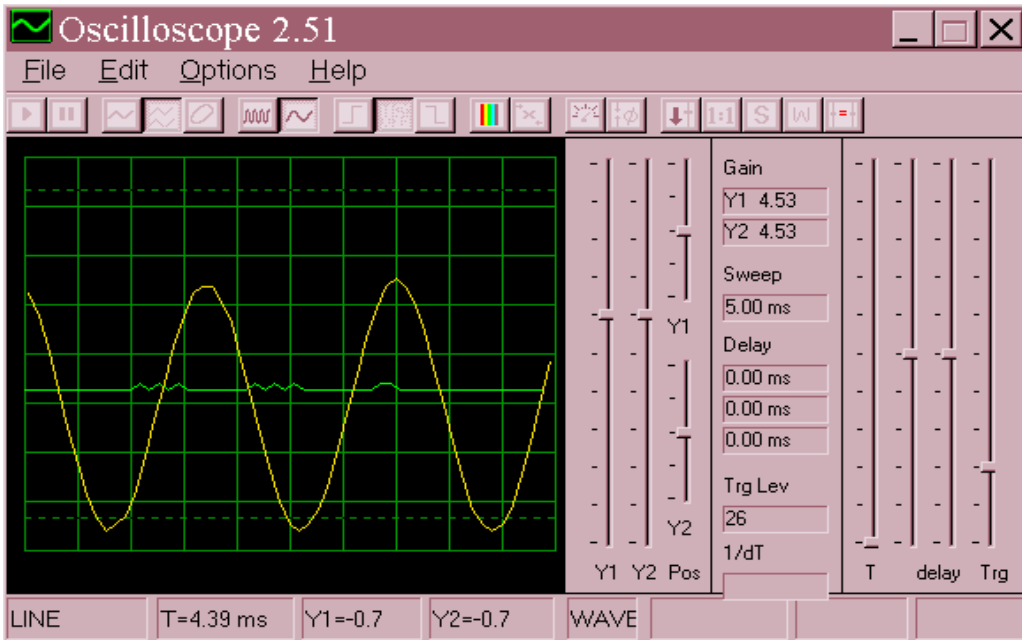
<i>Communications</i>	
Baud	9600
Bits	8
Stop bits	1
Parity	None
<i>Sine Wave, Square Wave, Triangular Wave</i>	
Frequency range	20Hz to 7812Hz
Available Frequencies(in Hz)	Frequency from 20Hz to 84Hz in steps of 1 Frequency from 84Hz-102Hz in steps of 2 From 102-114Hz in steps of 3 From 114-134Hz in steps of 4 From 134-144Hz in steps of 5 From 144-162Hz in steps of 6 169,177,186,195,205,217,229,244,260, 279,300,325,355,390,434,488,558,651, 781,976,978,1116,1302,1562,1953,1955, 2232,2604,3125,3906,3908,4464,5208, 6250,7812 If the frequency set by the serial command is not available then the next closest one is selected from the above table.
<i>Serial Command</i>	
For Sine Wave	SXXXX<CR> where X denotes digit in the frequency value (ASCII data format)
For Square Wave	QXXXX<CR>
For Triangular Wave	TXXXX<CR>
Example	S0050 followed by carriage return, generates sine wave @ 50Hz

Project number 231

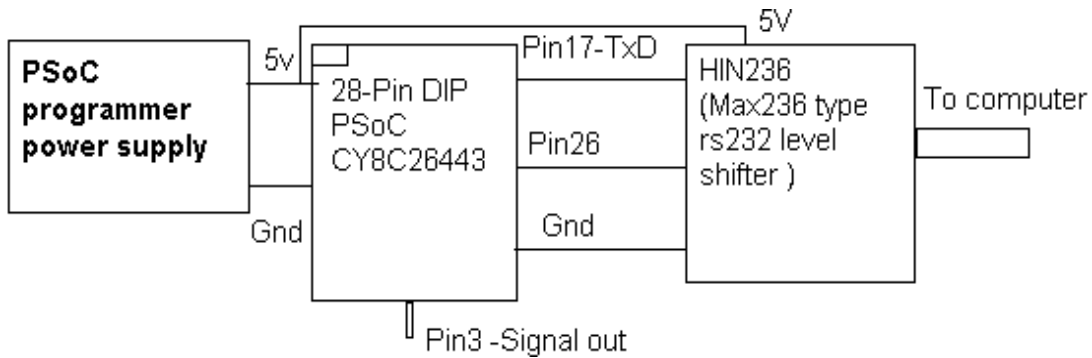
The picture below shows the project board. The board on the left is a RS232 level shifter connected to the computer and the board on the right is a PSoC PUP board with a ZIF socket.



The picture below shows a PC soundcard based scope capturing the 580Hz waveform generated.



Schematic



Design

The CPU runs at 12MHz. An 8-bit **counter** is used to provide a clock for the UART. The input clock for the **counter** is obtained by dividing the 24V1 by 16 ($24\text{MHz}/16$). The 8-bit **counter**, DBA03 is set to run at 78.9kHz by setting the counter value to 19. This amounts to dividing the input clock by 19. Each time the counter reaches 0 it is automatically reloaded. A compare value for the counter is set to 9 which sets up a duty cycle at the output of approximately 50%. The UART is set up to operate at a 9600-Baud Rate by the **counter** output frequency. Baud Rate is determined by the UART input clock frequency divided by 8 Parity is set to NONE for the block. UART Tx output is connected to Pin 17 and Rx input is connected to pin 26.

The **Dac** generates different waveforms using timings from the interrupt generated by the **timer** and is available on pin3. The input clock for the **timer** is 24V2. This is obtained by dividing 24V1 by 3 ($24\text{MHz}/16/3$). The **timer** is set to run at a frequency depending on the period value in the period register. The period value is changed as per the required frequency (sample no. per period of the waveform is also changed to get different frequencies). The period is automatically reloaded when the counter reaches 0 or when the **timer** is enabled from the disabled state. When the counter reaches 0 a **timer** interrupt is generated. On each interrupt updates the DAC.