

DESIGN OF A DIGITAL READ OUT  
BASED ON CYPRESS MICROSYSTEMS'  
PSOC MICROCONTROLLER SERIES

PROJECT #221

A PAPER PRESENTED TO CIRCUIT CELLAR  
IN FULFILLMENT OF THE REQUIREMENTS  
FOR THE PSOC DESIGN CONTEST

CIRCUIT CELLAR

2002

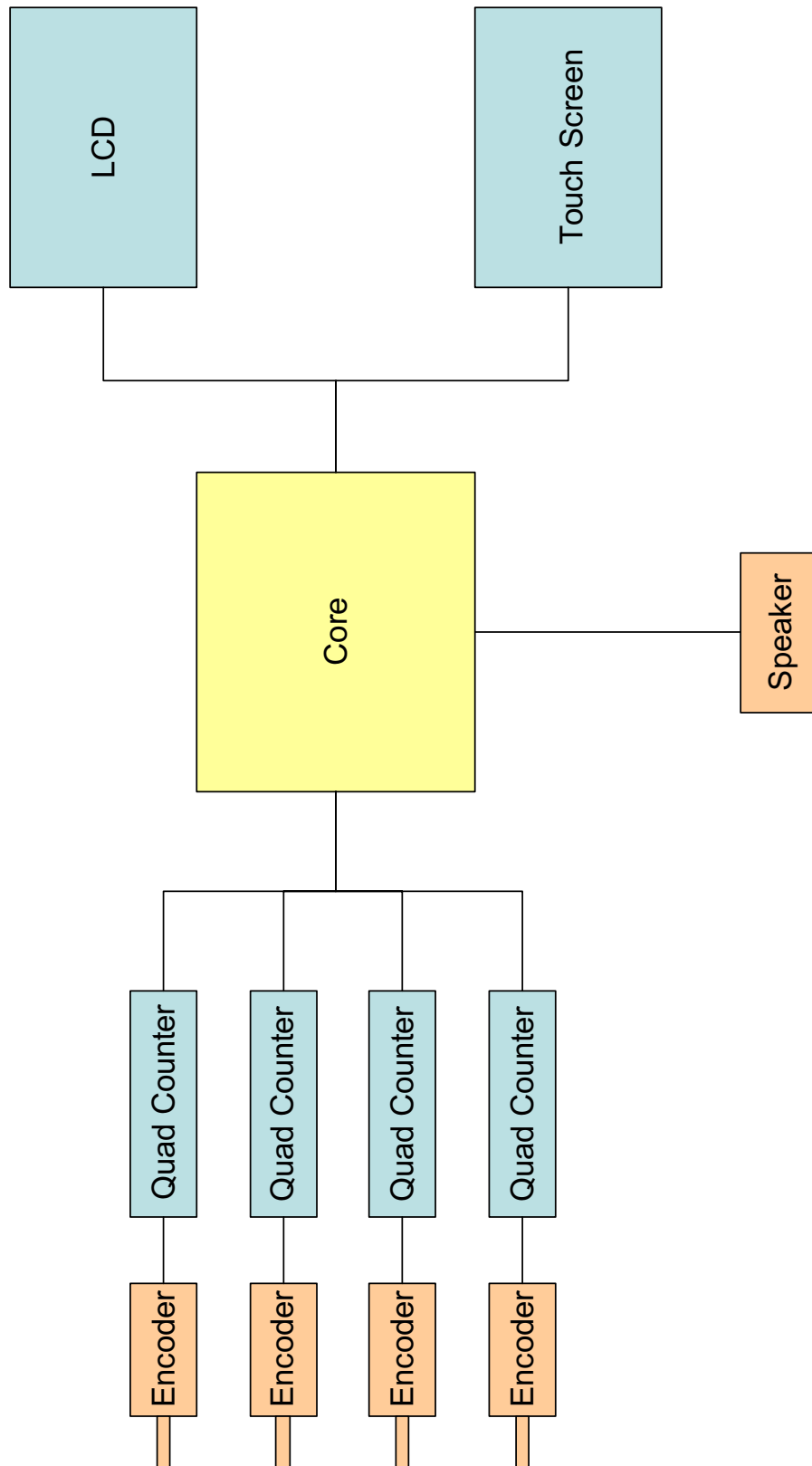
## ABSTRACT

Although advanced computer numerical control (CNC) machines exist for machining precision parts, a vast number of mechanical parts are still machined by hand. When producing prototypes through hand machining, high precision is still necessary. This precision is difficult to find in machines designed for milling by hand. The axis controls on the machines present all sorts of opportunities for slipping and backlash. These machines can be made to incorporate a greater deal of precision through the use of a Digital Read Out. This project outlines the development of a Digital Read Out designed using the Cypress MicroSystems CY8CXXX series microcontroller. The Digital Read Out incorporates measurement readouts for up to four axes through a robust user interface. The axes all have individual controls for clearing and setting each specific measurement value. The project uses a 320x200 backlit LCD display and an analog touch screen creating simple user operation. All the core components are from the CY8CXXX microcontroller family.

The project relies on optical encoders placed on each axis of the mill. Four quadrature decoders, implemented in CY8C25122-24PI, are used. The core microcontroller, a CY8C26443-24PI interfaces to the quadrature decoders using an SPI communication bus. The LCD display is used to show graphics and text to the user creating a large bright interface. It is connected to the core microcontroller through an 8-bit data bus. The analog touch screen reads button-press input from the user, and is interfaced through an internal analog mux. This paper describes the operation and design of the Digital Read Out designed for this project. The hardware, or electronic system is discussed. Code examples are shown to explain the software control system in the core controller



# BLOCK DIAGRAM



# APPENDIX A SCHEMATICS

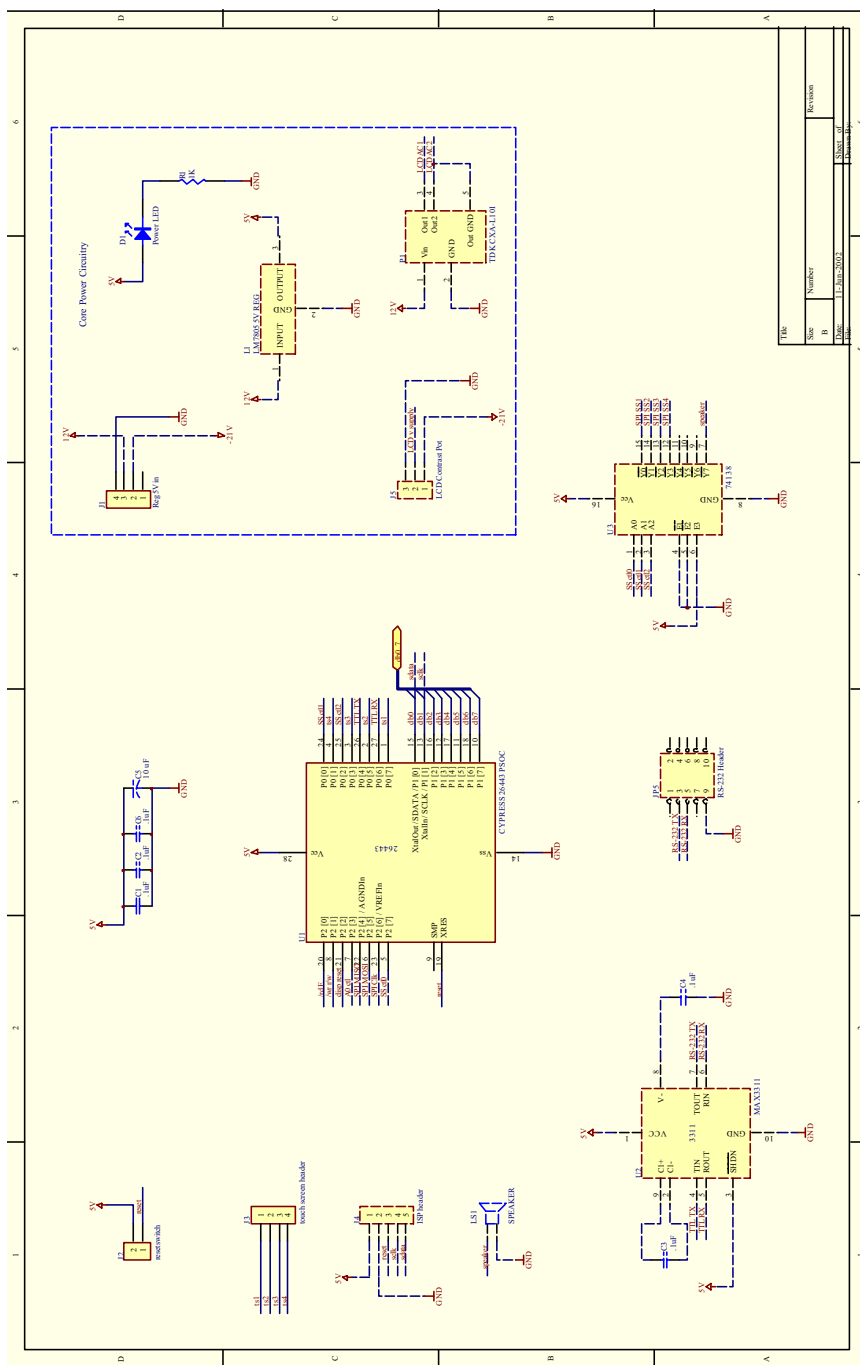


Figure A-1: Core schematic



